



Docket No.: 247953US2S

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

ATTORNEYS AT LAW

RE: Application Serial No.: 10/762,459

Applicants: Yoshiaki TAKEUCHI, et al.

Filing Date: January 23, 2004

For: ASYNCHRONOUS PSEUDO SRAM AND ACCESS
METHOD THEREFOR

Group Art Unit: 2824

Examiner: NGUYEN, T.

SIR:

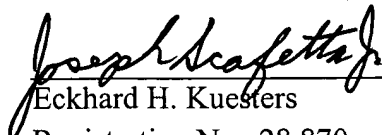
Attached hereto for filing are the following papers:

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Our check in the amount of \$0.00 is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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DOCKET NO: 247953US2S



IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
YOSHIAKI TAKEUCHI, ET AL. : EXAMINER: NGUYEN, T.
SERIAL NO: 10/762,459 :
FILED: JANUARY 23, 2004 : GROUP ART UNIT: 2824
FOR: ASYNCHRONOUS PSEUDO SRAM :
AND ACCESS METHOD THEREFOR

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant acknowledges with appreciation the indication of allowability of the claimed invention. In response to the Examiner's Statement of Reasons for Allowance in the Notice of Allowance of October 5, 2005, Applicant respectfully submits the following comments.

In the Examiner's Statement of Reasons for Allowance on page 4 of the Notice of Allowance mailed October 5, 2005, paragraph 4 states in part:

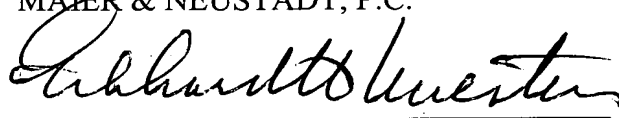
The prior art of record further fail to disclose an access method for a semiconductor integrated circuit device, in combination with other cited limitations, comprising when the transition of the row address or the column address latch and the second column address latch to respectively latch, after an end operation of the memory cell array, a row address and a column address detected, causing the second row address that are currently latched by the first row address latch and the first column address latch; and executing the next cycle operation of the memory cell array in accordance with the addresses latched by the second row address latch and the second column address latch. as recited in claim 21.

The above-quoted Examiner's Statement of Reasons for Allowance of Claim 21 does not correspond with the features recited in Claim 21. Accordingly, Claim 21 should not be construed based on the inaccurate description in the Examiner's Reasons.

Consequently, Applicant respectfully submits that the inaccuracy in the Examiner's Reasons for Allowance may create a cloud on the validity of the patent. Applicant therefore respectfully requests the Examiner issue a corrected Notice of Allowance.

Respectfully submitted,

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